PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference P775PC00	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
International application No. PCT/DK 03/00404	International filing date *(day/month/year)* 18.06.2003	Priority date *(day/month/year)* 19.06.2002
International Patent Classification (IPC) or both national classification and IPC H03L7/085		
Applicant R & C Holding ApS et al.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 5 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 5 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the opinion
   - II ☐ Priority
   - III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - VI ☐ Certain documents cited
   - VII ☐ Certain defects in the international application
   - VIII ☐ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
16.01.2004	13.12.2004
Name and mailing address of the international preliminary examining authority: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized Officer Nicolaucig, A Telephone No. +49 89 2399-7670

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/DK 03/00404

I. Basis of the report

1. With regard to the **elements** of the international application *(Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17))*:

Description, Pages

1-49 as published

Claims, Numbers

1-18 received on 28.10.2004 with letter of 25.10.2004

Drawings, Sheets

1/14-14/14 as published

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

These elements were available or furnished to this Authority in the following language: , which is:

- ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).
- ☐ the language of publication of the international application (under Rule 48.3(b)).
- ☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

- ☐ contained in the international application in written form.
- ☐ filed together with the international application in computer readable form.
- ☐ furnished subsequently to this Authority in written form.
- ☐ furnished subsequently to this Authority in computer readable form.
- ☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
- ☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

- ☐ the description, pages:
- ☐ the claims, Nos.:
- ☐ the drawings, sheets:

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)).

   (Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)

6. Additional observations, if necessary:

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1-18
	No:	Claims	
Inventive step (IS)	Yes:	Claims	1-18
	No:	Claims	
Industrial applicability (IA)	Yes:	Claims	1-18
	No:	Claims	

2. Citations and explanations

   see separate sheet

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1 Reference is made to the following documents:

D1: US-A-6046643
D2: US-A-6075387

2 The document D1 is regarded as being the closest prior art to the subject-matter of claim 1, and shows (the references in parentheses applying to this document):

a method (see figure) for determining a phase error (output of D/A) in response to a first signal (fref, clock input of ACCU2) and a second signal (clock input of ACCU1), said method comprising the steps of:

generating a first reoccurring trigger event (rising/falling edge on clock input of ACCU2) in response to the first signal,

generating a second reoccurring trigger event (rising/falling edge on clock input of ACCU1) in response to the second signal,

incrementing (col. 3, l. 18-20) a first phase value by a first predetermined increment value (aref) when the first trigger event occurs to obtain a first accumulated phase value (output of ACCU2) represented by a binary number,

incrementing a second phase value (col. 3, l. 17-18) by a second predetermined increment value when the second trigger event occurs to obtain a second accumulated phase value (output of ACCU1) represented by a binary number, and

calculating or determining (through H1, H3 and D/A) said phase error based on obtained first and second accumulated phase values, said phase error being represented by a binary number (output of D/A) or one or more analogue signals (input of D/A).

2.1 The subject-matter of claim 1 differs from this known method for determining a phase

error in that

said method further comprises the steps of
resetting the most significant bit of the first accumulated phase value and the most significant bit of the second accumulated phase value when the most significant bit of both said first accumulated phase value and said second accumulated phase value are simultaneously 1.

2.2 The subject-matter of claim 1 is therefore novel (Article 33(2) PCT).

2.3 The problem to be solved by the present invention may be regarded as avoiding an overflow of the accumulated phase and making it easier to obtain a difference between the two accumulated phase values.

2.4 The solution to this problem proposed in claim 1 of the present application is considered as involving an inventive step (Article 33(3) PCT) for the following reasons:

there is no hint in D1 or D2 to the problem of overflowing of the accumulated phase value nor to the proposed solution. The person skilled in the art would not arrive to such a solution without exercising an inventive step.

2.5 The same arguments apply mutatis mutandis to independent claim 8, defining corresponding phase-locked loop, and independent claim 14, defining corresponding phase comparator, so that they also meet the requirements of the PCT with respect to novelty and inventive step.

2.6 Claims 2-7, 9-13, 15-18 are dependent on claims 1, 8 or 14, and as such also meet the requirements of the PCT with respect to novelty and inventive step.

3 The subject-matter of claims 1-18 is industrially applicable.

CLAIMS filed in response to the first written opinion

1. A method for determining a phase error in response to a first signal and a second signal, said method comprising the steps of:

generating a first reoccurring trigger event in response to the first signal,

generating a second reoccurring trigger event in response to the second signal,

incrementing a first phase value by a first predetermined increment value when the first trigger event occurs to obtain a first accumulated phase value represented by a binary number,

incrementing a second phase value by a second predetermined increment value when the second trigger event occurs to obtain a second accumulated phase value represented by a binary number, and

calculating or determining said phase error based on obtained first and second accumulated phase values, said phase error being represented by a binary number or one or more analogue signals,

said method further comprising the steps of

resetting the most significant bit of the first accumulated phase value and the most significant bit of the second accumulated phase value when the most significant bit of both said first accumulated phase value and said second accumulated phase value are simultaneously 1.

2. A method according to claim 1, wherein the phase error is represented by one or more an analogue signals.

3. A method according to claim 2, said method further comprising the steps of:

performing a first logic bit by bit AND operation of the first accumulated phase value and the inverted second accumulated phase value, and generating a first analogue representation of said first logic bit by bit AND operation, and

performing a second logic bit by bit AND operation of the second accumulated phase value and the inverted first accumulated phase value, and generating a second analogue representation of said second logic bit by bit AND operation.

4. A method according to claim 3, wherein the calculation of the phase error comprises generating one or more analogue phase error signal based on the sec-

ond analogue representation of the second logic bit by bit AND operation and the first analogue representation of the first logic bit by bit AND operation.

5. A method according to claim 4, wherein the calculation of the phase error comprises performing an analogue subtraction of the second analogue representation from the first analogue representation.

6. A method according to any one of the claims 1-5, wherein two equal bits are reset whenever these bits are 1 at the same time.

7. A method according to any one of the claims 1-6, said method comprising the step of frequency dividing the first signal and/or the second signal, whereby the generation of the first and/or second reoccurring trigger event is performed in response to the frequency divided first and/or second signal, respectively.

8. A phase-locked loop comprising:

a voltage controlled oscillator for generating an output signal and having a frequency control input for controlling the frequency of the output signal, and

a phase comparator for deriving a control signal from a phase error detected in response to the received output signal and a reference signal, said control signal being coupled to the frequency control input of said voltage controlled oscillator, wherein the phase comparator includes:

a first accumulator adapted to add a first predefined phase step value to a first accumulated phase value in response to a reoccurring event in the reference signal,

a second accumulator adapted to add a second predefined phase step value to a second accumulated phase value in response to a reoccurring event in the received output signal, and

means or arithmetic means for determining the phase error from the obtained first and second accumulated phase values,

said phase comparator further including a first reset means for the most significant bit of the first accumulator, a second reset means for the most significant bit of the second accumulator, and a third AND-means, where the output of said third AND-means is connected to said first and said second reset means of said first and said second accumulator, where the most significant bit of said first accumulator is connected to a first non-inverting input of said third AND-means, and where the

most significant bit of said second accumulator is connected to a second non-inverting input of said third AND-means.

9. A phase-locked loop according to claim 8, wherein the phase comparator includes a converter circuit having:

means for performing a first logic bit by bit AND operation of the output of the first accumulator and the inverted output of the second accumulator, and for generating a first analogue representation of said first logic bit by bit AND operation, and

means for performing a second logic bit by bit AND operation of the output of the second accumulator and the inverted output of the first accumulator, and for generating a second analogue representation of said second logic bit by bit AND operation.

10. A phase-locked loop according to claim 9, wherein the converter circuit comprises current mode logic circuits giving a current output for a two input AND operation, said current output being used for generating an analogue representation for a bit by bit AND operation.

11. A phase-locked loop according to claim 9 or 10, wherein the arithmetic means are adapted to obtain one or more analogue phase error signals based on the second analogue representation of the second logic bit by bit AND operation and the first analogue representation of the first logic bit by bit AND operation.

12. A phase-locked loop according to claim 11, wherein the arithmetic means comprises subtraction means being adapted for performing an analogue subtraction of the second analogue representation from the first analogue representation.

13. A phase-locked loop according to any one of the claims 8-12, further comprising a divider for dividing the frequency of the output signal, whereby the received output signal received by the phase comparator is a frequency-divided output signal.

14. A phase comparator for carrying out the method in accordance to claim 1-7, wherein the first signal is a reference signal and the second signal is an input signal, said phase comparator including:

a first accumulator adapted to add a first predefined phase step value to a first accumulated phase value in response to a reoccurring event in said reference signal,

a second accumulator adapted to add a second predefined phase step value to a second accumulated phase value in response to a reoccurring event in said input signal, and

means or arithmetic means for determining the phase error based on the second accumulated phase value and the first accumulated phase value,

said phase comparator further including a first reset means for the most significant bit of the first accumulator, a second reset means for the most significant bit of the second accumulator and a third AND-means, where the output of said third AND-means is connected to said first and said second reset means of said first and said second accumulator, where the most significant bit of said first accumulator is connected to a first non-inverting input of said third AND-means, and where the most significant bit of said second accumulator is connected to a second non-inverting input of said third AND-means.

15. A phase comparator according to claim 14, wherein the phase comparator includes a converter circuit having:

means for performing a first logic bit by bit AND operation of the output of the first accumulator and the inverted output of the second accumulator, and for generating a first analogue representation of said first logic bit by bit AND operation, and

means for performing a second logic bit by bit AND operation of the output of the second accumulator and the inverted output of the first accumulator, and for generating a second analogue representation of said second logic bit by bit AND operation.

16. A phase comparator according to claim 15, wherein the converter circuit comprises current mode logic circuits giving a current output for a two bit AND operation, said current output being used for generating an analogue representation for a bit by bit AND operation.

17. A phase comparator according to claim 15 or 16, wherein the arithmetic means are adapted to obtain one or more analogue phase error signals based on

the second analogue representation of the second logic bit by bit AND operation and the first analogue representation of the first logic bit by bit AND operation.

18. A phase comparator according to claim 17, wherein the arithmetic means comprises subtraction means being adapted for performing an analogue subtraction of the second analogue representation from the first analogue representation.